

SPECIFICATION FOR APPROVAL

ITEM : 5.6" TFT LCD MODULE

MODEL NO : BS - 560U

CUSTOMER : _____

DATE : _____

NO : _____

DESCRIBED	CHECKED	APPROVED

CONTENTS

1. GENERAL FEATURES	----- PAGE 3
2. SPECIFICATIONS	----- PAGE 4
3. DIMENSIONS	----- PAGE 5
4. BLOCK DIAGRAM	----- PAGE 6
5. CONNECTION DIAGRAM	----- PAGE 7
6. DATA SHEETS FOR MAIN COMPONENTS	----- PAGE 8

1. GENERAL FEATURES

FEATURES

- 1-1. ACTIVE MATRIX COLOR TFT LCD MODULE
- 1-2. COMPACT SIZE (DIAGONAL 5.6 INCH)
- 1-3. LOW POWER CONSUMPTION
- 1-4. BEST QUALITY IMAGE
- 1-5. COMPOSITE REGULATED VIDEO INPUT SIGNAL

APPLICATIONS

- 2-1. COLOR VIDEO DOOR ENTRY SYSTEM
- 2-2. CCTV MONITOR
- 2-3. CAR REAR VIEW MONITOR
- 2-4. SURVEILLANCE SYSTEM

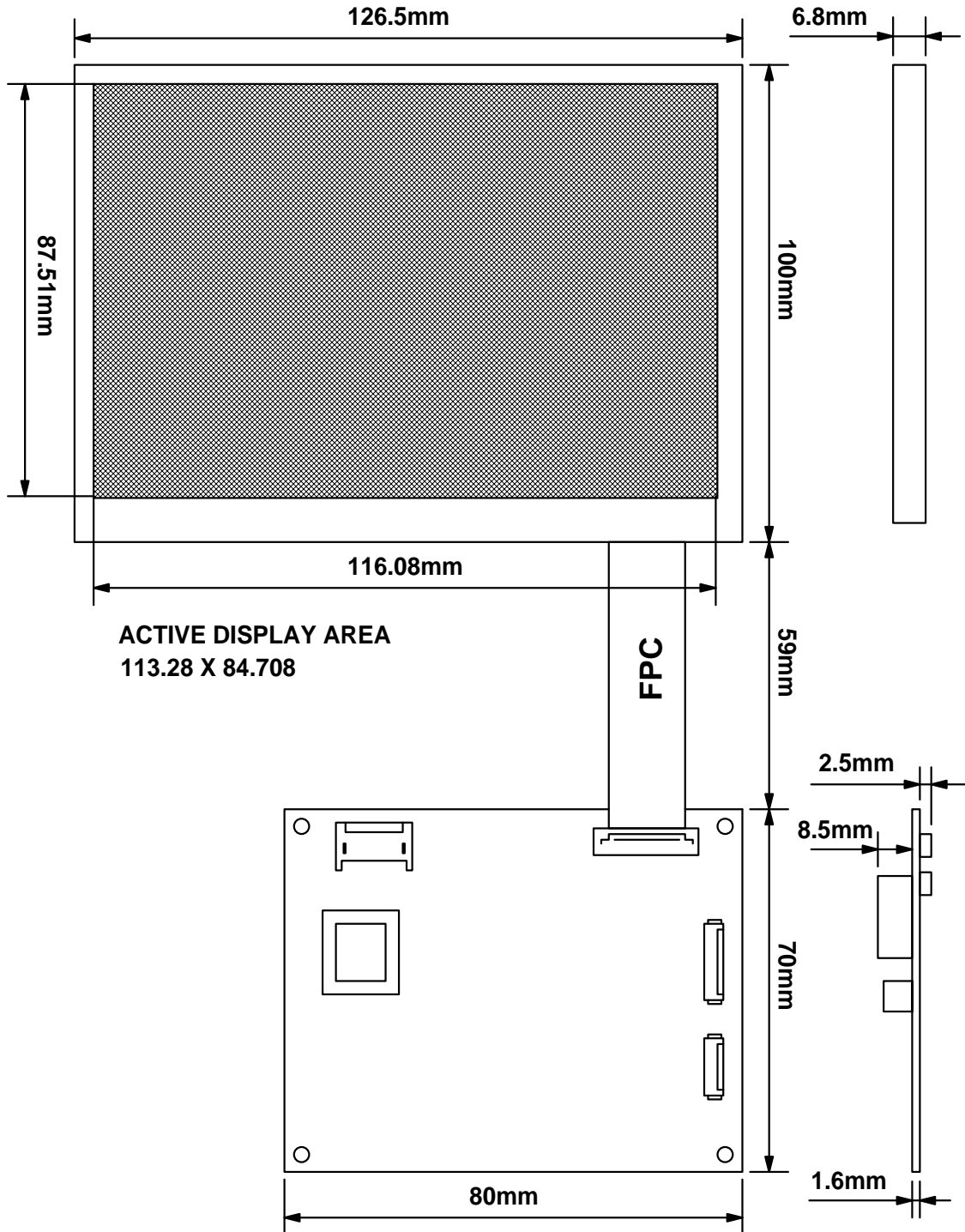
2. SPECIFICATIONS

1	DISPLAY SIZE	DIAGONAL 5.6 INCH	REMARK
2	DOT PITCH	0.362(V) * 0.118(H)	
3	DOT FORMAT	234(V) * 960(H)	
4	PIXELS ARRANGEMENT	RGB VERTICAL STRIPE	
5	DISPLAY METHOD	TFT ACTIVE MATRIX SYSTEM	
6	INPUT SIGNAL	PAL/NTSC (OPTION)	
7	INPUT SIGNAL LEVEL	1.0Vp-p, 75 Ohm	
8	VIEWING ANGLE	TOP : 10 DEG BOTTOM : 30 DEG LEFT & LIGHT : 45 DEG	NOTE 1
9	BRIGHTNESS	TYP. 300(cd)	
10	OPERATING TEMPERATURE	0 ~ 60 95%RH	
11	STORAGE TEMPERATURE	-25 ~ 80 95%RH	
12	INPUT VOLTAGE	DC12V ± 5%, 550mA ± 10%	
13	DIMENSION	126.5(W) * 100(H) * 6.8(D)	NOTE 2
14	WEIGHT	APPX. 180(g)	

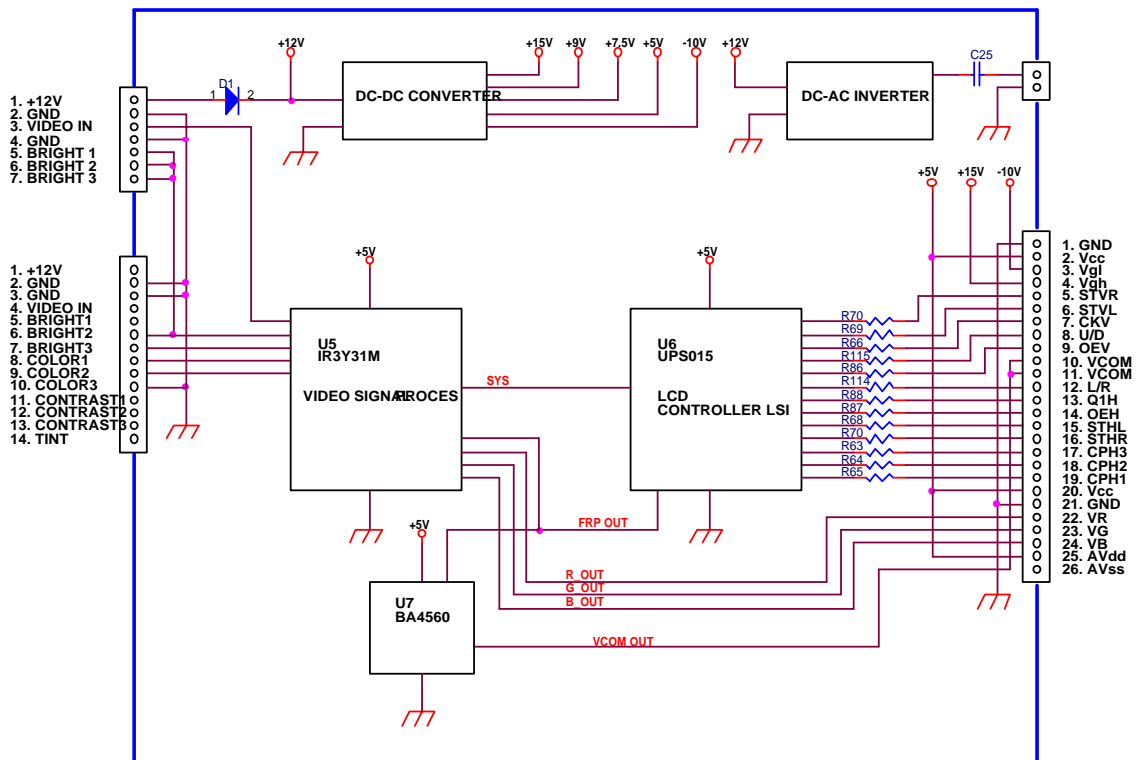
NOTE 1. REFER TO THE ATTACHED PANEL SPEC A056DN01.

NOTE 2. THE DIMENSIONS ARE WITHOUT DRIVE BOARD.

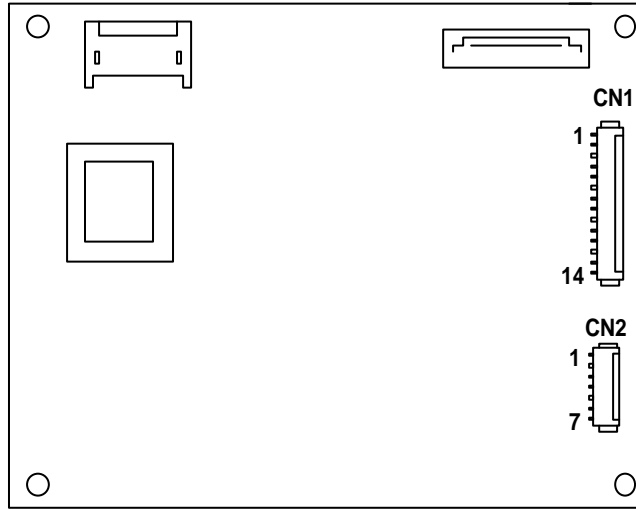
3. DEMENSIONS



4. BLOCK DIAGRAM

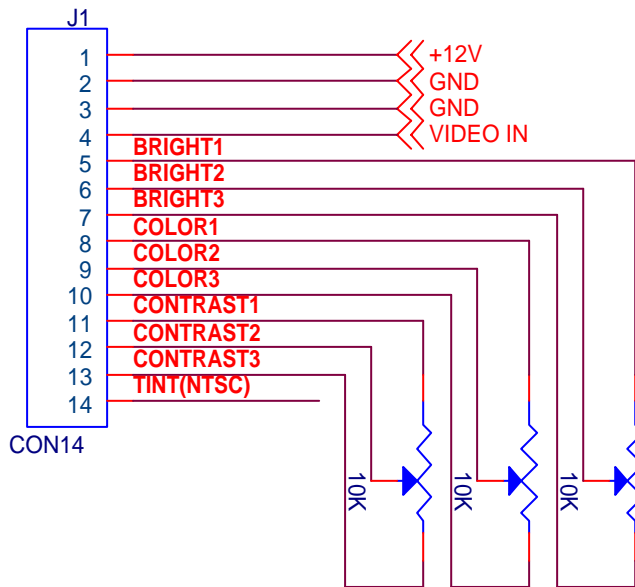


5. CONNECTION DIAGRAM



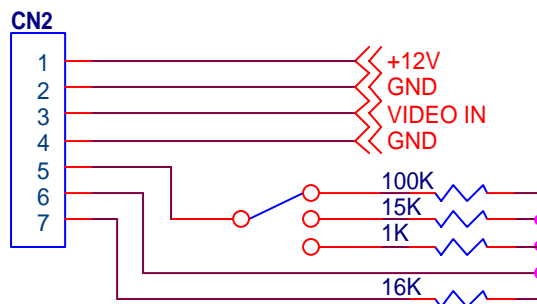
A TYPE - OUTSIDE VOLUME CONTROL (CN1)

- 1. BRIGHT
- 2. COLOR
- 3. CONTRAST
- 4. TINT - NTSC ONLY



B TYPE - OUTSIDE VOLUME CONTROL (CN2)

- 1. BRIGHTNESS ONLY



6. DATA SHEETS FOR MAIN COMPONENTS

6-1. LCD PANEL: A056DN01

Version	3
Total pages	19
Date	2002.Apr.09

Product Specification

5.6" color TFT-LCD module

Model name: A056DN01

Original model name: UP056D01

(.....) Preliminary Specification

() Final Specification

Record of Revision

Version	Revise Date	Page	Content		
1	01/Nov./1999	-	First draft		
2	11/Sep./2000	3	A.7. Change weight(g) => (180 ±20) 145 ±10		
		6	3.a. Change V_{GLAC} of power supply =>(5)(Typ.) 5(Typ.)		
			Change V_{GLDC} of power supply => V_{GLDC} V_{GL-H}		
			Change remark of V_{GL-H} => DC component of V_{GL} High level of V_{GL}		
			Change V_{CAC} of VCOM =>(5)(Typ.) 5(Typ.)		
			Change V_{CDC} of VCOM =>TBD (Min.) 1.30(Min.) TBD(Typ.) 1.40(Typ.) TBD (Max.) 1.50(Max.)		
			3.b. Change I_{GH} of current for driver =>(0.26)(Typ.) 0.2(Typ.) (0.8)(Max.) 0.8(Max.)		
			Change I_{GL} of current for driver =>(-0.41)(Typ.) -0.5(Typ.) (-1)(Max.) -1.0(Max.)		
			Change I_{CC} of current for driver =>(6.5)(Typ.) 4.0(Typ.) (12)(Max.) 8.0(Max.)		
			Change I_{BD} of current for driver =>(10)(Typ.) 12(Typ.) (20)(Max.) 20(Max.)		
			Change I_{VCOM} of current for driver =>TBD(Typ.) 10(Typ.) TBD (Max.) 18(Max.)		
			3.c. Change V_L => TBD - (Min.) (580) 470(Typ.) (638) 528(Max.)		
			Change I_L => (5) 5.9(Min.) (7) 6.1(Max.)		
		Change F_L => - 80(Max.)			
		Change V_S => (930) - (Typ.) Remark: Note 1,3,5 (1100) -(Typ.) Remark: Note 2,3,5 (1150) 650(Max.) Remark: Note 1,3,5 (1150) 910(Max.) Remark: Note 2,3,5			
		3	09/Apr./2002		Change the model name due to a new effective company_AU

Contents:

A. Physical specification. P3

B. Electrical specifications. P4

 1. Pin assignment. P4

 a. TFT-LCD panel driving section. P4

 b. Backlight driving section. P5

 2. Absolute maximum ratings. P5

 3. Electrical characteristics. P6

 a. Typical operating conditions. P6

 b. Current consumption. P6

 c. Backlight driving conditions. P6

 4. AC Timing. P7

 a. Timing conditions. P7

 b. Timing diagram. P7

C. Optical specifications. P8

D. Reliability test items. P10

E. Packing form P11

Appendix:

Fig.1 Outline dimension of TFT-LCD module. **P12**
Fig.2 Sampling clock timing. **P13**
Fig.3 Horizontal display timing range. **P14**
Fig.4-(a) Horizontal timing. **P15**
Fig.4-(b) Detail horizontal timing. **P16**
Fig.5 Vertical shift clock timing. **P17**
Fig.6-(a) Vertical timing (From up to own).. **P18**
Fig.6-(b) Vertical timing (From down to up) **P19**

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution(dot)	960(W) ×234(H)	
2	Active area(mm)	113.3(W) ×84.7(H)	
3	Screen size(inch)	5.6(Diagonal)	
4	Dot pitch(mm)	0.118(W) ×0.362(H)	
5	Color configuration	R. G. B. stripe	
6	Overall dimension(mm)	126.5(W) ×100(H) ×6.8(D)	Note 1
7	Weight(g)	145 ±10	

Note 1: Refer to Fig. 1

B. Electrical specifications

1.Pin assignment

a. TFT-LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V _{CC}	I	Supply voltage of logic control circuit for scan driver	
3	V _{GL}	I	Negative power for scan driver	
4	V _{GH}	I	Positive power for scan driver	
5	STVR	I/O	Vertical start pulse	Note 1
6	STVL	I/O	Vertical start pulse	Note 1
7	CKV	I	Shift clock input for scan driver	
8	U/D	I	Up/Down scan control input	Note 1,2
9	OEV	I	Output enable input for scan driver	
10	VCOM	I	Common electrode driving signal	
11	VCOM	I	Common electrode driving signal	
12	L/R	I	Left/Right scan control input	Note 1,2
13	Q1H	I	Analog signal rotate input	
14	OEH	I	Output enable input for data driver	
15	STHL	I/O	Start pulse for horizontal scan line	Note 1
16	STHR	I/O	Start pulse for horizontal scan line	Note 1
17	CPH3	I	Sampling and shifting clock pulse for data driver	
18	CPH2	I	Sampling and shifting clock pulse for data driver	
19	CPH1	I	Sampling and shifting clock pulse for data driver	
20	V _{CC}	I	Supply voltage of logic control circuit for data driver	
21	GND	-	Ground for logic circuit	
22	VR	I	Alternated video signal input(Red)	
23	VG	I	Alternated video signal input(Green)	
24	VB	I	Alternated video signal input(Blue)	
25	AV _{DD}	I	Supply voltage for analog circuit	
26	AV _{SS}	-	Ground for analog circuit	

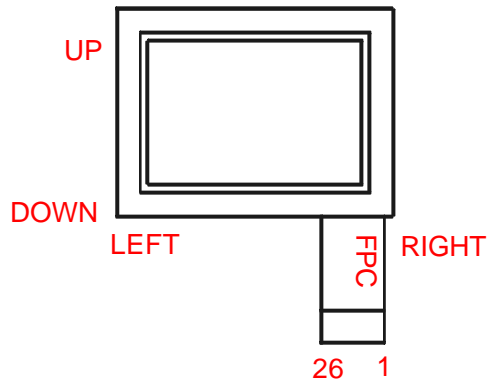
Note 1: Selection of scanning mode (please refer to the following table)

Setting of scan control input		IN/OUT state For start pulse				Scanning direction
U/D	L/R	STVR	STVL	STHR	STHL	
GND	V _{CC}	OUT	IN	OUT	IN	From up to down, and from left to right.
V _{CC}	GND	IN	OUT	IN	OUT	From down to up, and from right to left.
GND	GND	OUT	IN	IN	OUT	From up to down, and from right to left.
V _{CC}	V _{CC}	IN	OUT	OUT	IN	From down to up, and from left to right.

IN: Input; OUT: Output.

Note 2 : Definition of scanning direction.

Refer to figure as below:



b. Backlight driving section(Refer to Fig. 1)

No.	Symbol	I/O	Description	Remark
1	HI	I	Power supply for backlight unit (High voltage)	
2	GND	-	Ground for backlight unit	

2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V _{CC}	GND=0	-0.3	7	V	
	AV _{DD}	AV _{SS} =0	-0.3	7	V	
	V _{GH}	GND=0	-0.3	18	V	
	V _{GL}		-15	0.3	V	
	V _{GH} - V _{GL}		-	31	V	
Input signal voltage	V _i		-0.3	AV _{DD} +0.3	V	Note 1
	V _I		-0.3	V _{CC} +0.3	V	Note 2
	V _{COM}		-2.9	5.2	V	
Operating temperature	T _{opa}		0	60		Ambient temperature
Storage temperature	T _{stg}		-25	80		Ambient temperature

Note 1: VR, VG, VB

Note 2: STHL, STHR, Q1H, OEH, L/R, CPH1~CPH3, STVR, STVL, OEV, CKV, U/D.

3. Electrical characteristics

a. Typical operating conditions (GND=AVss=0V, Note 5)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply	V _{CC}	4.8	5	5.2	V	
	AV _{DD}	4.8	5	5.2	V	
	V _{GH}	14.3	15	15.7	V	
	V _{GLAC}	-	5	-	Vp-p	AC component of V _{GL} . Note 1
	V _{GL_H}	-10.5	-10	-9.5	V	High level of V _{GL} .
Video signal Amplitude (VR, VG, VB)	V _{iA}	AV _{SS} +0.4	-	AV _{DD} -0.4	V	Note 2
	V _{iAC}	-	3	-	V	AC component
	V _{iDC}	-	AV _{DD} /2	-	V	DC component
VCOM	V _{CAC}	-	5	-	Vp-p	AC component, Note 3
	V _{CDC}	1.3	1.4	1.5	V	DC component
Input Signal voltage	H Level	V _{IH}	0.8V _{CC}	-	V _{CC}	Note 4
	L Level	V _{IL}	0	-	0.2V _{CC}	

Note 1: The same phase and amplitude with common electrode driving signal(VCOM).

Note 2: Refer to Fig.4-(a)

Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 4: STHL, STHR, Q1H, OEHL, L/R, CPH1~CPH3, STVR, STVL, OEVL, CKV, U/D.

Note 5: Be sure to apply GND, V_{CC} and V_{GL} to the LCD first, and then apply V_{GH}.

b. Current consumption (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for driver	I _{GH}	V _{GH} =15V	-	0.2	0.8	mA	
	I _{GL}	V _{GL} =-10V	-	-0.5	-1	mA	
	I _{CC}	V _{CC} =5V	-	4	8	mA	
	I _{DD}	AV _{DD} =5V	-	12	20	mA	
	I _{VCOM}	V _{CAC} =5V	-	10	18	mA	
	I _{L11}	-	-10	-	10	μA	Note 1

Note 1: Logic Input Leakage Current

c. Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V _L	-	470	528	Vrms	Note 3
Lamp current	I _L	5.9	6	6.1	mArms	
Frequency	F _L	-	60	80	kHz	Note 3,4
Lamp starting voltage	V _S	-	-	650	Vrms	Note 1,3,5
		-	-	910	Vrms	Note 2,3,5

Note 1: Ta = 25 .

Note 2: Ta = 0 .

Note 3: Reference value, correct value is subject to final backlight specification which will be decided in the future.

Note 4: The lamp frequency should be selected as different as possible from display horizontal synchronous signal to avoid interference.

Note 5: For starting the backlight unit, the output voltage of DC/AC's transformer should be larger than the maximum lamp starting voltage.

4. AC Timing

a. Timing conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_{r1}	-	-	60	ns	CPH1~CPH3
Falling time	t_{f1}	-	-	60	ns	CPH1~CPH3
Rising time	t_{r2}	-	-	120	ns	CKV
Falling time	t_{f2}	-	-	120	ns	CKV
High and low level pulse width	t_{CPH}	150	154	158	ns	CPH1~CPH3
CPH pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3
CPH pulse delay	t_{C12} t_{C23} t_{C31}	30	$t_{CPH}/3$	$t_{CPH}/2$	ns	CPH1~CPH3
STH setup time	t_{SUH}	20	-	-	ns	STHR,STHL
STH hold time	t_{HDH}	20	-	-	ns	STHR,STHL
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STHR,STHL
STH period	t_H	61.5	63.5	65.5	μs	STHR,STHL
OEH pulse width	t_{OEH}	-	7	-	t_{CPH}	OEH
Sample and hold disable time	t_{DIS1}	-	55	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	27	-	t_{CPH}	OEV
CKV pulse width	t_{CKV}	-	41	-	t_{CPH}	CKV
Clean enable time	t_{DIS2}	-	16	-	t_{CPH}	
Horizontal display start	t_{SH}	-	0	-	$t_{CPH}/3$	
Horizontal display timing range	t_{DH}	-	960	-	$t_{CPH}/3$	
STV setup time	t_{SUV}	400	-	-	ns	STVL,STVR
STV hold time	t_{HDV}	400	-	-	ns	STVL,STVR
STV pulse width	t_{STV}	-	-	1	t_H	STVL,STVR
Horizontal lines per field	t_V	256	262	268	t_H	Note 1
Vertical display start	t_{SV}		3	-	t_H	
Vertical display timing range	t_{DV}		234	-	t_H	
VCOM rising time	t_{rCOM}		-	5	μs	
VCOM falling time	t_{fCOM}		-	5	μs	
VCOM delay time	t_{DCOM}		-	3	μs	
RGB delay time	t_{DRGB}		-	1	μs	

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b. Timing diagram

Please refer to the attached drawing, from Fig.2 to Fig.6.

C. Optical specification (Note 1,Note 2, Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	Tr	=0 °	-	15	30	Ms	Note 4,6
	Fall	Tf		-	20	40		
Contrast ratio		CR	At optimized viewing angle	100	150	-		Note 5,6
Viewing angle	Top		CR 10	10	-	-	deg.	Note 6,7
	Bottom			30	-	-		
	Left			45	-	-		
	Right			45	-	-		
Brightness			=0 °	250	300	-	nit	Note 8
White chromaticity		X	=0 °	0.25	0.30	0.35		Note 8
		Y	=0 °	0.30	0.35	0.40		

Note 1. Ambient temperature =25 . And lamp current $I_L = 6mArms$.

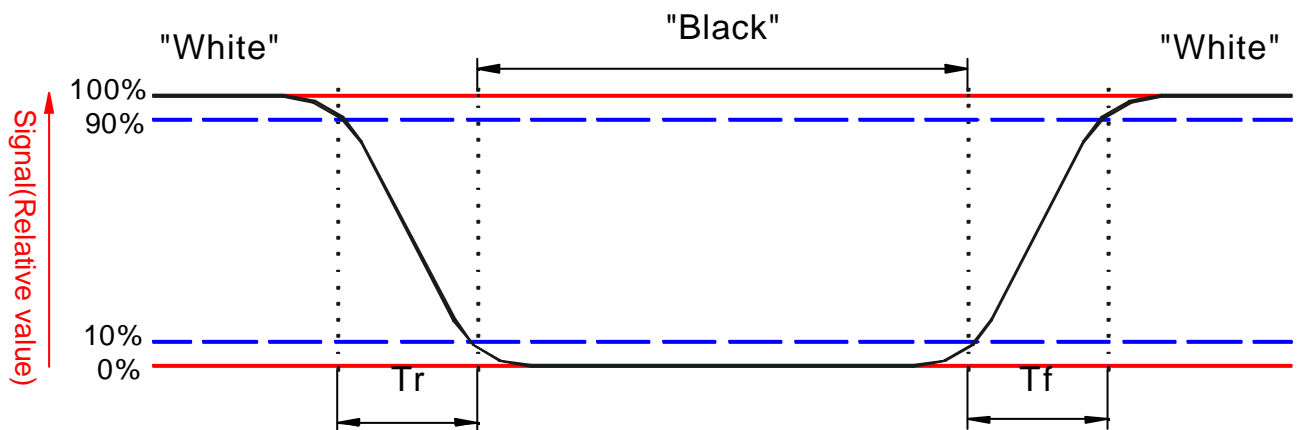
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a viewing cone of 1 by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photodetector are measured when the input signals are changed from “black” to “white” (falling time)and from “white” to “black” (rising time),respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photodetector output when LCD is at "White" state}}{\text{Photodetector output when LCD is at "Black" state}}$$

Note 6. White $V_i = V_{i50} \mp 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

" \mp " means that the analog input signal swings in phase with COM signal.

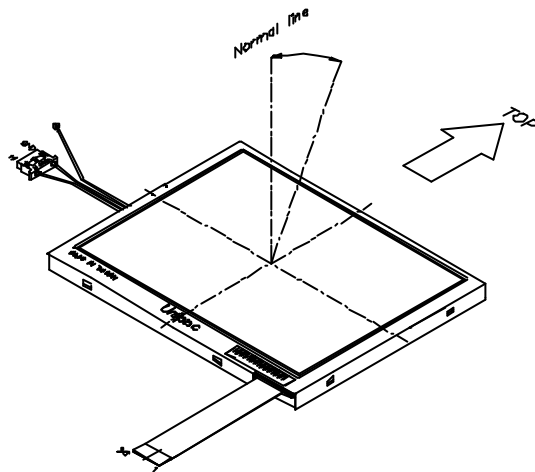
" \pm " means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:

Refer to figure as below.



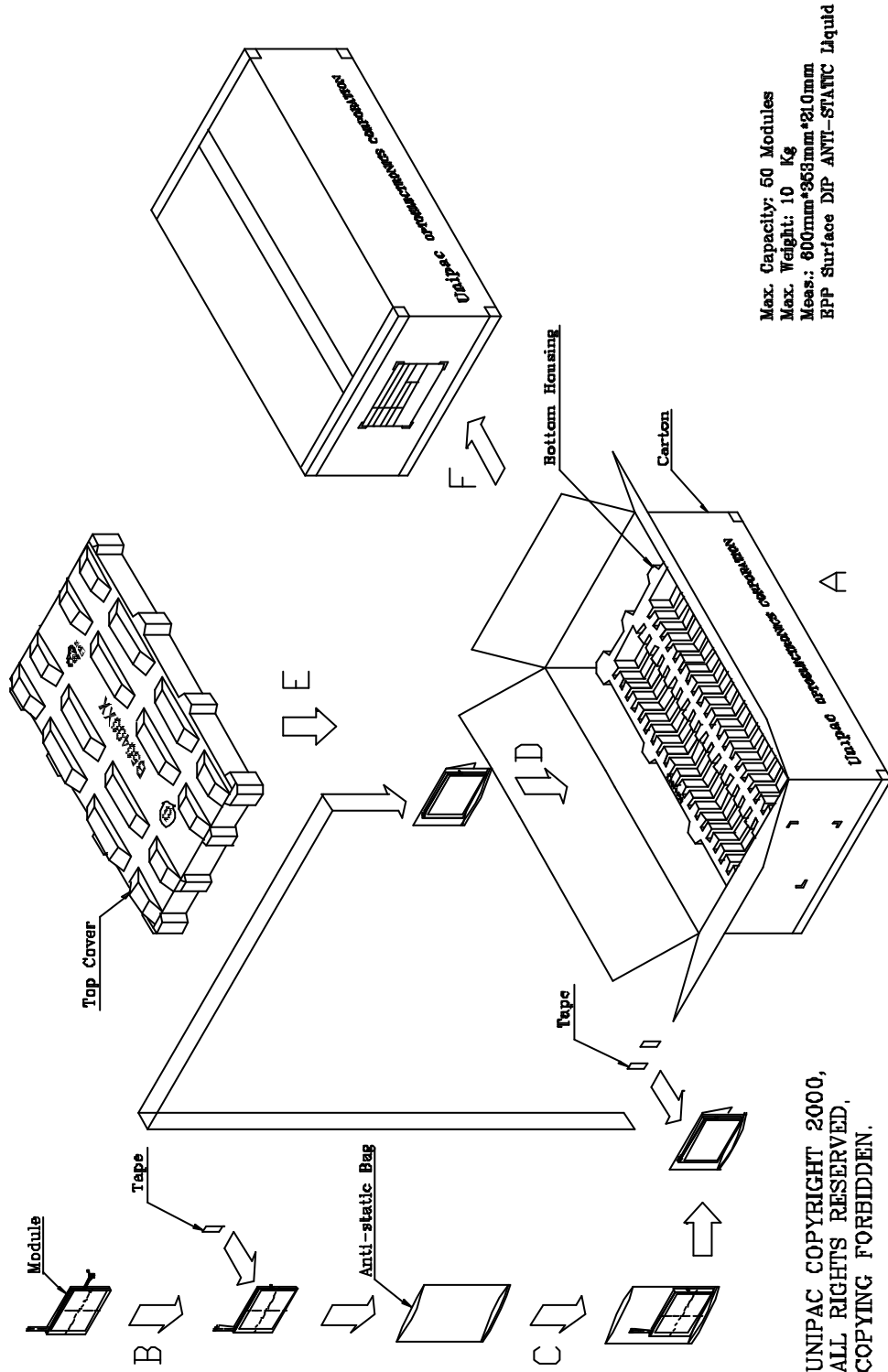
Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80 240Hrs	
2	Low temperature storage	Ta= -25 240Hrs	
3	High temperature operation	Ta= 60 240Hrs	
4	Low temperature operation	Ta= 0 240Hrs	
5	High temperature and high humidity	Ta= 60 , 95% RH 240Hrs	Operation
6	Heat shock	-25 ~80 /50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	JIS C7021, A-10 condition A
9	Mechanical shock	100G , 6ms, ±X, ±Y, ±Z 3 times for each direction	JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: 0.015G ² /Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: (60)cm 1 corner. 3 edges. 6 surfaces	JIS Z0202

Note: Ta: Ambient temperature.

E.Packing form



Max. Capacity: 50 Modules
 Max. Weight: 10 Kg
 Meas.: 800mm*368mm*210mm
 EPP Surface DIP ANTI-STATIC Liquid

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- NOTES:
 1. General tolerance is ± 0.30 .
 2. The bending radius of FPC should be larger than 0.6.
 3. Unit : mm.
 4. Glass thickness = 0.7mm

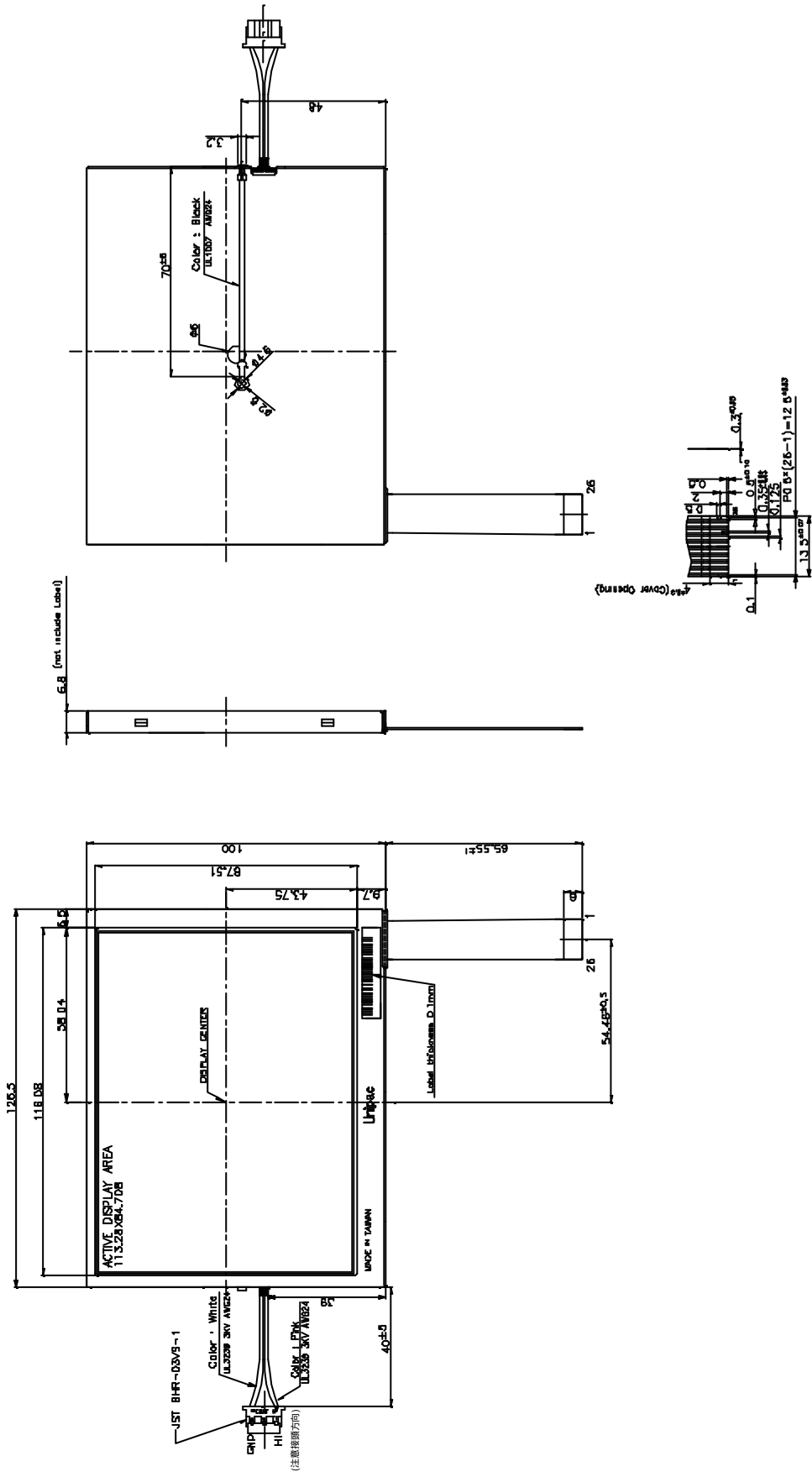


Fig. 1 Outline dimensio of TFT-LCD module

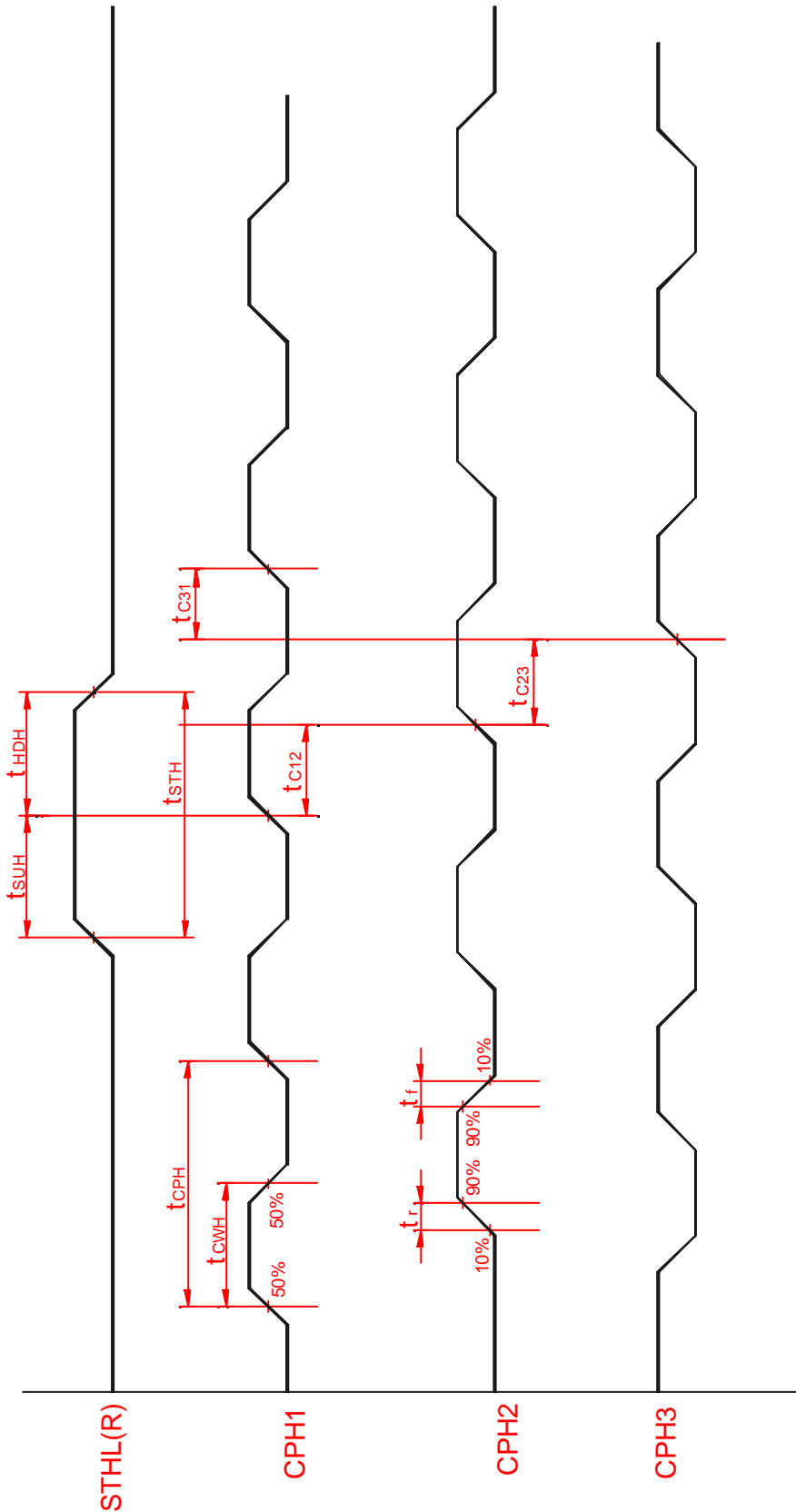


Fig. 2 Sampling clock timing

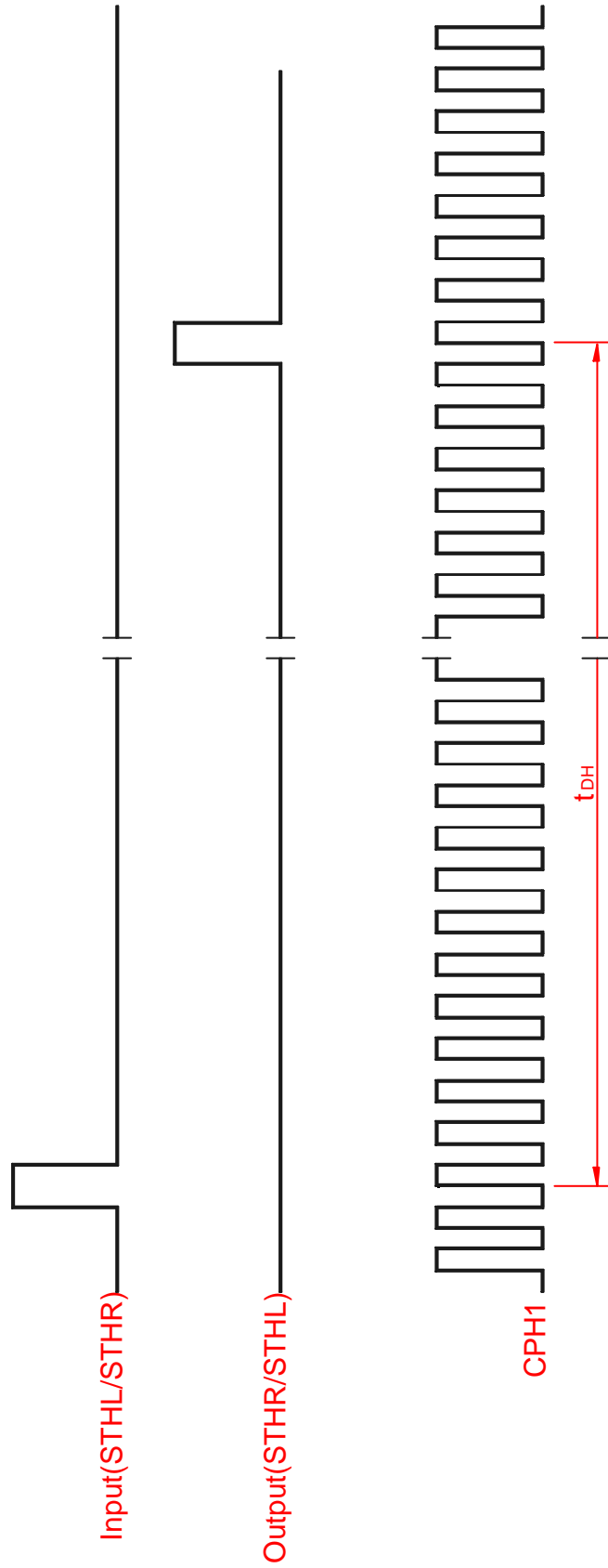


Fig. 3 Horizontal display timing range

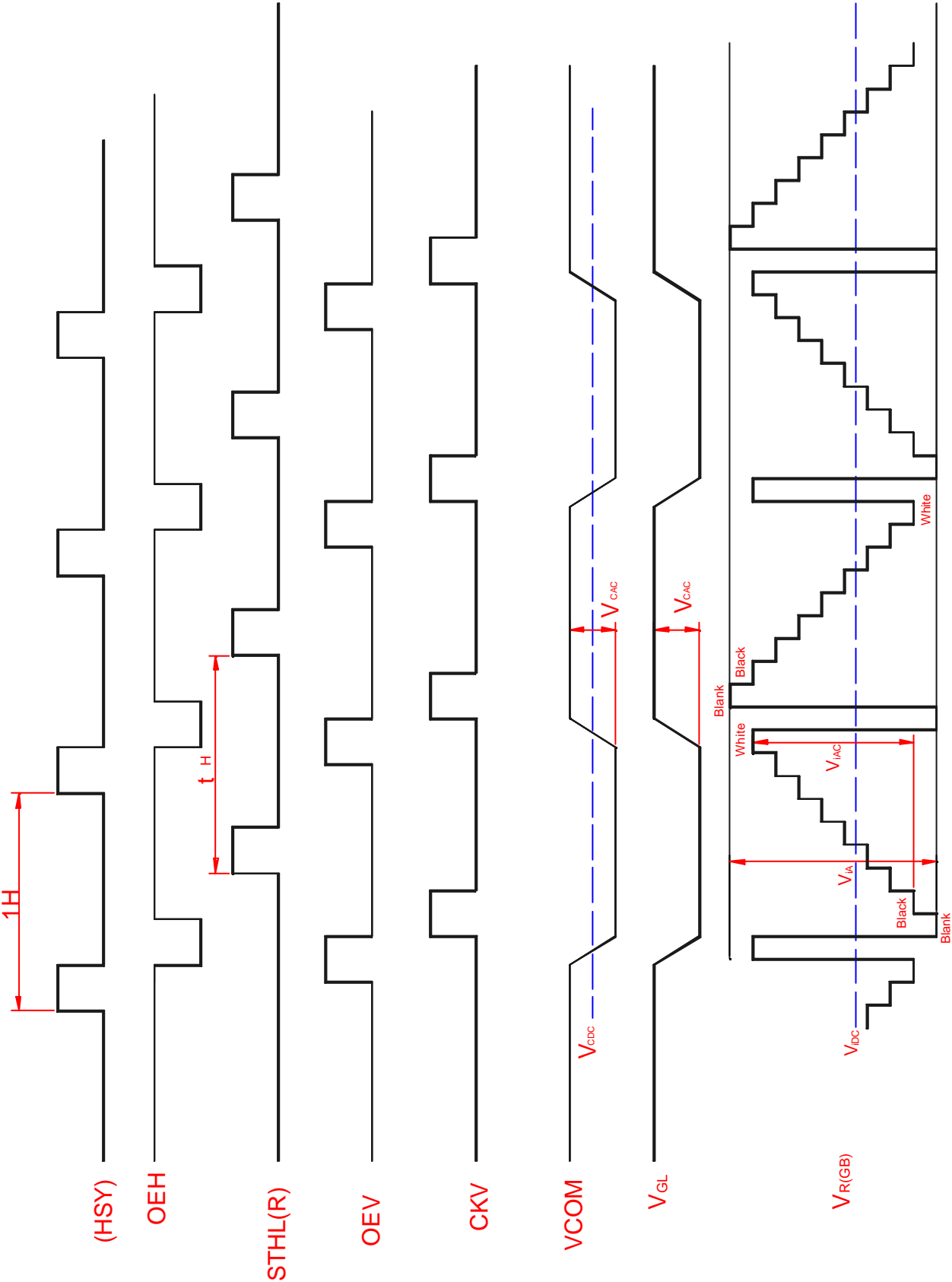
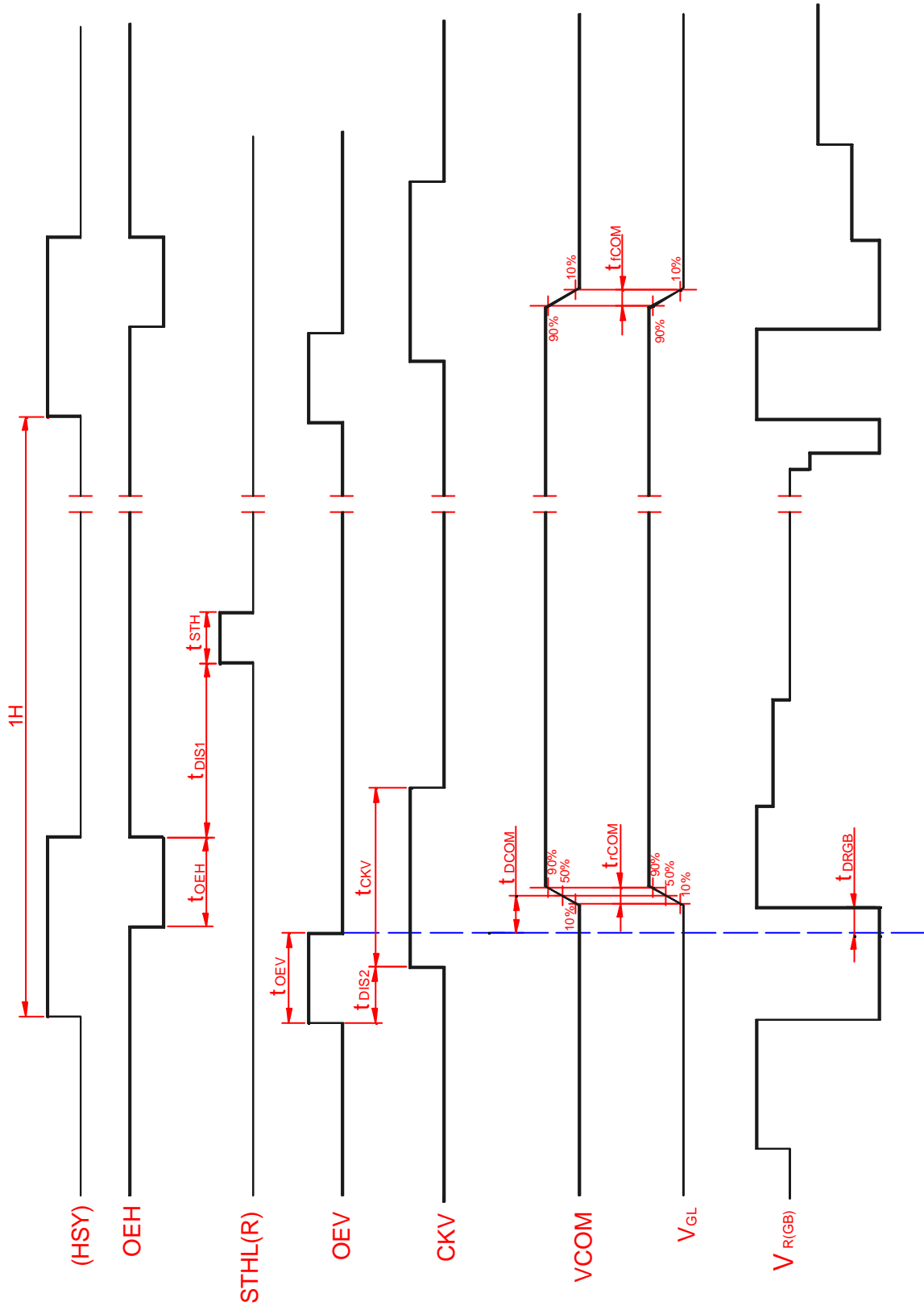


Fig.4-(a) Horizontal timing



Note: The falling edge of OEV should be synchronized with the falling edge of OEH

Fig. 4-(b) Detail horizontal timing

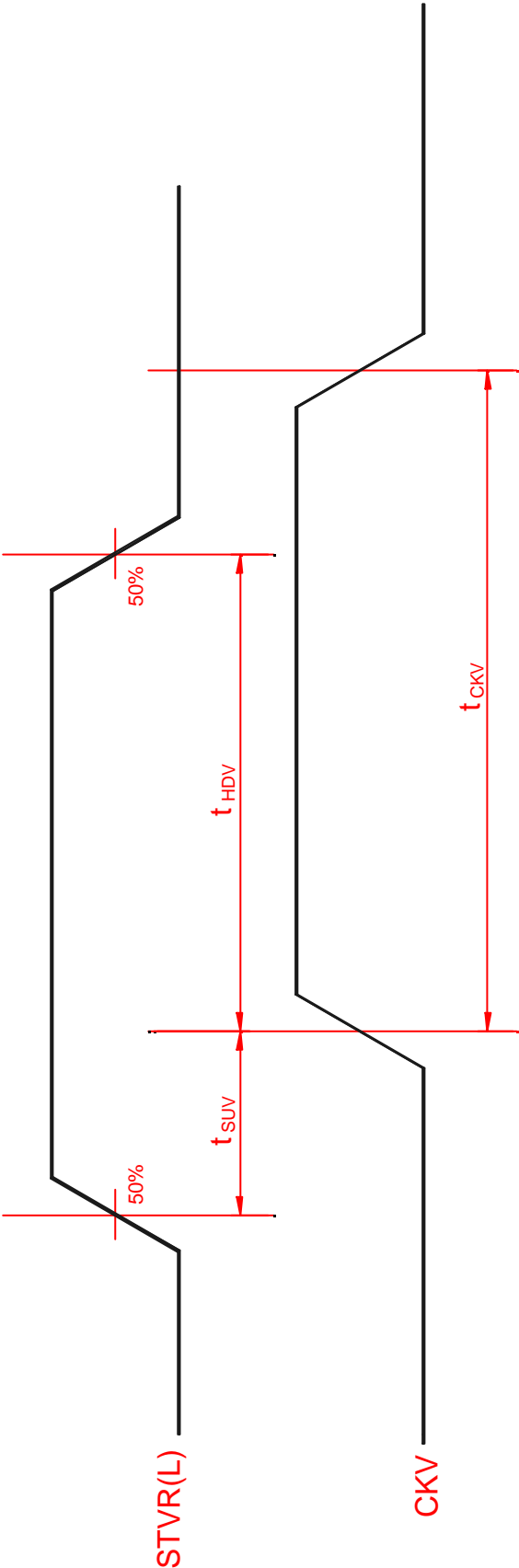


Fig.5 Vertical shift clock timing

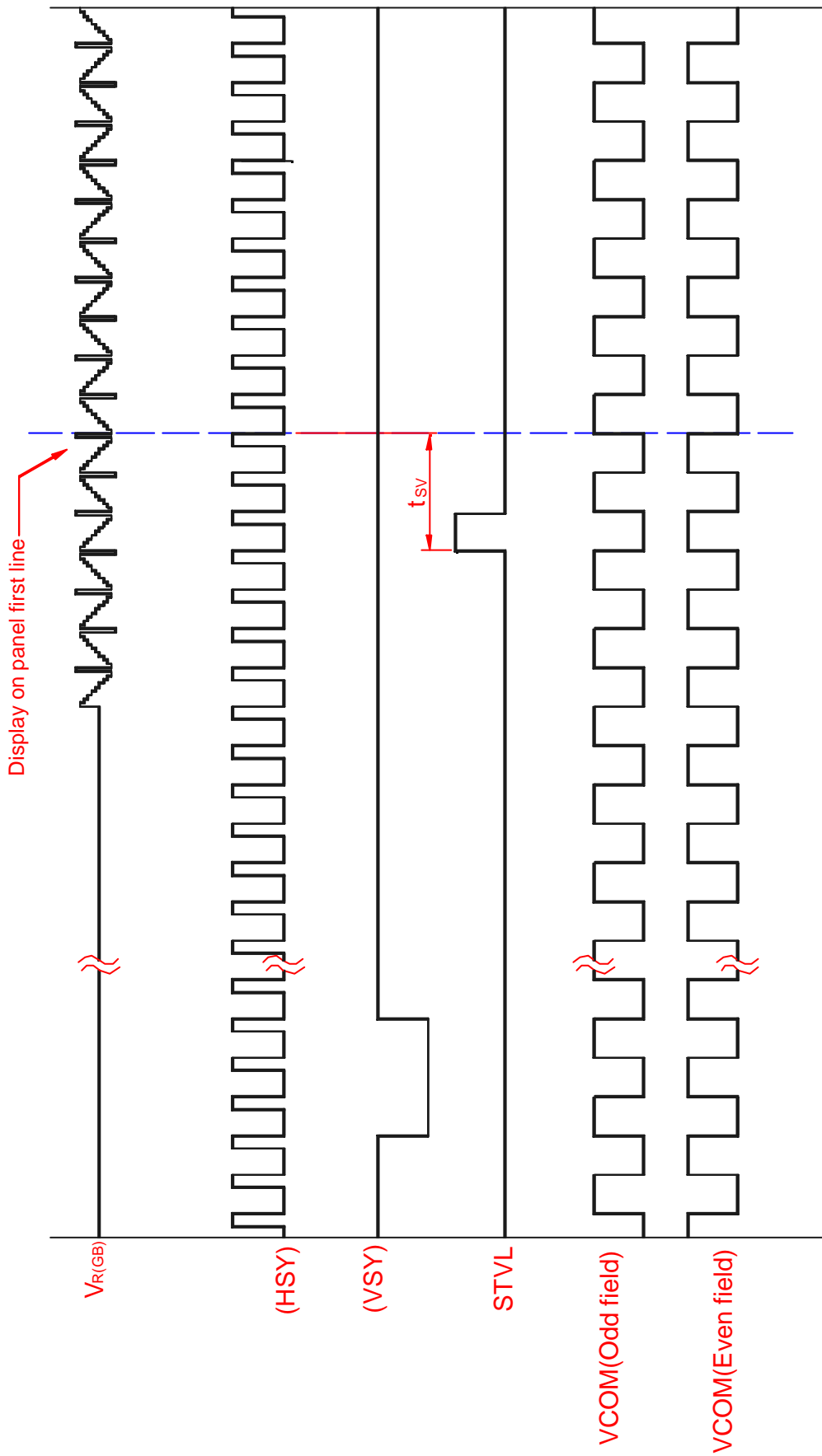


Fig.6-(a) Vertical timing (From up to down)

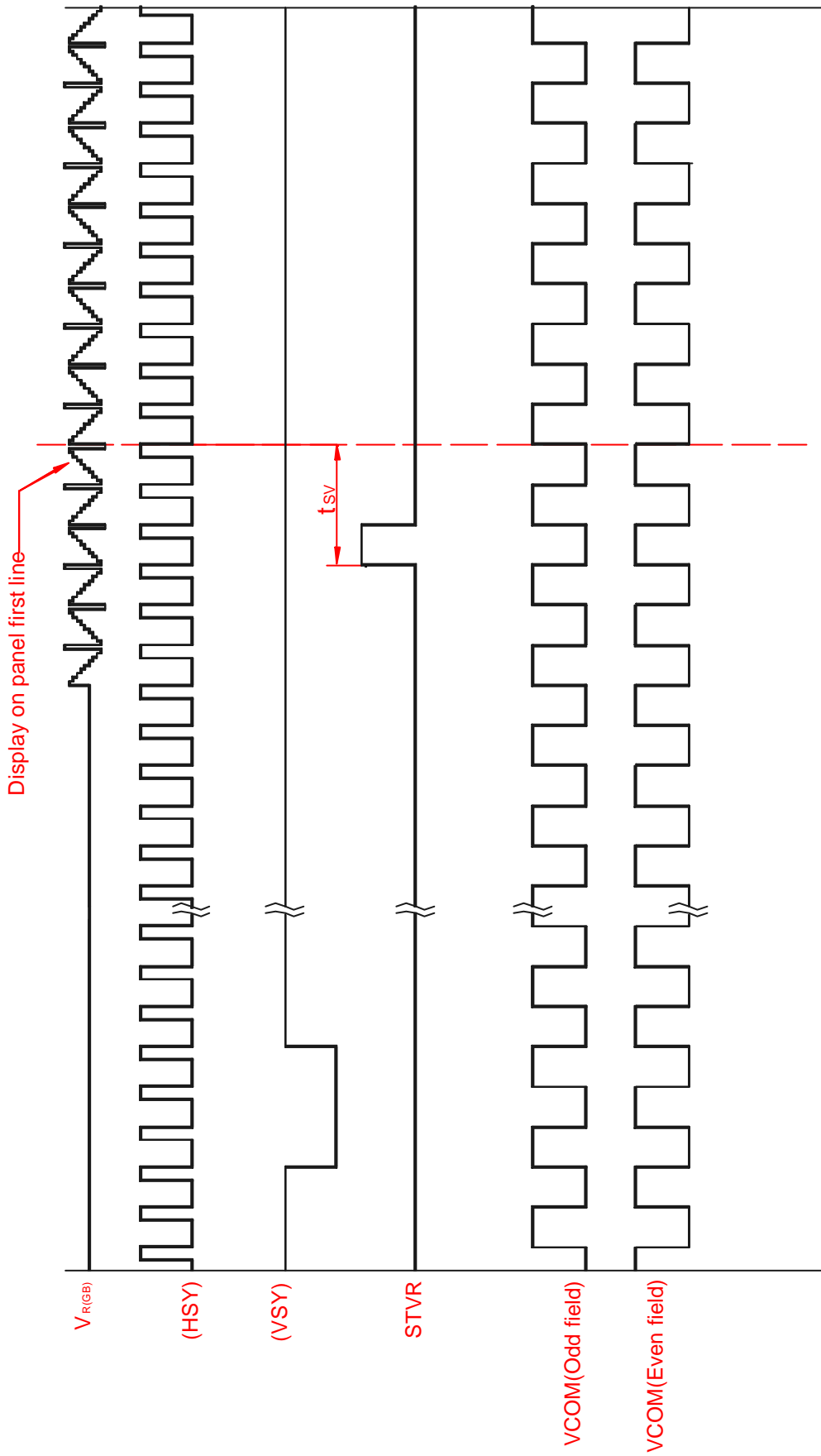


Fig.6-(b) Vertical timing (From down to up)